REMARKS/ARGUMENTS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and the following reasons. By way of this Amendment and Reply, Claims 1, 3-6, 8, 9, 13, 14, 16-19, 21, 22, 26, 28, 29, 33, 42, and 52 have been amended. No new matter has been added by way of these amendments. Claims 35-41 were previously canceled. Claims 1-34 and 42-61 are currently pending in this application.

Though the above claim amendments are being made after a final rejection, Applicants respectfully request entry of these claim amendments. The claim amendments have been made to clarify the claim language and to correct minor typographical and grammatical errors. As such, the claim amendments do not require a new search or further consideration by the Examiner. In addition, the claim amendments place the application in better condition for appeal.

I. Interview Summary

Applicant thanks the Examiner for the courtesy extended during the telephone interview on December 10, 2009.

During the telephone interview, Applicant's representative Feng Ma (Reg. No. 58,192) discussed three issues with Examiner Bello, summaries of which are provided below. No agreement was reached during the interview.

1. The Williams '157 reference relied upon in the final Office Action does not qualify as prior art. Applicant has previously presented this argument. However, the Examiner has not addressed this issue, and has not addressed the parent patent from which Williams '157 is a continuation-in-part. Accordingly, Applicant requests that the finality of the Office Action be withdrawn and that this issue be addressed in an Office Action unless the Examiner finds Applicant's amendments and the following arguments place all the claims in condition for allowance.

2. In the final Office Action, the Examiner referred to a number of elements of the Williams '949 reference as the grouping trench, including numeral references 64, 68, and 70. However, elements 64 and 70 are not "trenches," and trenches 68 do not extend from the second side of the substrate 62 as claimed.

The Examiner responded that in Fig. 6 of Williams '949, reference numeral 69 points to "trenches," and that the devices in Williams '157 are "grouped," and therefore the combined references teach a "grouping trench."

Applicant noted that the reference numerals 69 in Williams '949 actually refer to the optical devices themselves, and the indentations over the optical devices 69 (which are actually optical windows for these optical devices) cannot be interpreted as the "grouping trench" as claimed.

3. In the final Office Action, the Examiner asserted that elements 50, 70, 72 of Williams '949 are the "common substrate" for the optical devices. However, element 70 is a flowable epoxy hardener material and element 72 is a standoff grid. Element 50 is a separate ASIC substrate flip-chip bonded to the optical devices 69.

The Examiner responded that the phrase "substrate" can be construed as any common platform.

II. Claim Rejections Under 35 U.S.C. § 103(a)

In Section 2 of the final Office Action, Claims 1-34 and 42-61 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,763,157 to Williams et al. (hereinafter "Williams '157") in view of U.S. Patent No. 6,614,949 to Williams et al. (hereinafter "Williams '949"). For at least the following reasons, the rejection is respectfully traversed.

As Applicant has previously noted, Williams '157 was filed on June 4, 2002, after the filing date (June 29, 2001) of the present application. Accordingly, Williams '157 may not be

used as prior art against the claims of the present application. Because Williams '157 is a continuation-in-part of its parent application (U.S. Patent No. 6,398,425), the PTO has the burden to show that the elements relied upon in Williams '157 find support in its parent application. Since the Examiner has not met this burden and has not responded to Applicant's repeated requests to address this issue in an Office Action, Applicant respectfully submits that the finality of the Office Action is improper and should be withdrawn.

To the extent that the Examiner finds support for the elements relied upon in Williams '157 in its parent application, Applicant requests that the Examiner clearly articulate the basis for this position in an Office Action.

Independent Claim 1 recites, among other elements, "at least two optical devices in a group are of a common device type formed on a first side of a common substrate," where "the group is separated from other groups by at least one grouping trench, and wherein the grouping trench extends into the common substrate from a second side of the common substrate opposite the first side of the common substrate." Independent Claims 13, 14, 26, 33, 42, and 52 each recite optical devices or lasers grown on a first side of a substrate or wafer and a grouping trench extending from a second side of the substrate or wafer.

In contrast, Williams '157 and Williams '949, whether considered separately or in a combination, fail to disclose, teach, or suggest at least this combination of elements.

The Examiner has conceded that Williams '157 fails to disclose, teach, or suggest the above-mentioned combination of elements, stating on page 2 of the final Office Action that "Williams '949 teaches that grouping trenches are well known in the art (column 4, lines 40-57)." In an attempt to overcome this deficiency, the Examiner asserted on page 3 of the Office Action that "Williams '949 teaches that grouping trenches are well known in the art (column 4, lines 40-57)." The cited portion of Williams '949 reads (with emphasis added as indicated by underlining):

> Referring particularly to FIG. 4, after completion of the electrical layer 66, but prior to application of the solder bumps 67, a grid or other suitable etch-mask pattern is applied to electrical layer 66 so as to divide the optical devices, or otherwise divide into subgroups the planned electrical connections and functionality of the several optical devices in the array, with an etched trench cavity system 68 that will later be an internal grid and protruding standoff structure. The etch-mask pattern may be designed to electrically isolate the respective optical devices or groups of devices with a uniform grid structure of intersecting walls, or to otherwise establish a distributed pattern of standoff structures, including walls, pillars and posts, between the optical devices or groups of devices, across what will be the optical face of chip 20 after the lapping and etching of the reverse side. The alternative distributed standoff structures may be useful in cases where the electrical isolation is not required or wanted.

Contrary to the Examiner's assertions, Williams '949 does not disclose, teach or suggest a "grouping trench," but instead teaches protruding standoff structures.

On page 3 of the final Office Action, the Examiner asserted that reference numerals 64, 68, and 70 in Figs. 4 and 5 of Williams '949 are "grouping trenches." Applicant respectfully disagrees.

As clearly shown in Figs. 4 and 5 of Williams '949 (reproduced below), elements 64 and 70 are not trenches. Element 70 is a "flowable epoxy hardener material," and element 64 is a "Gallium Arsenide layer" (see, e.g., col. 5, lines 20 and 31).

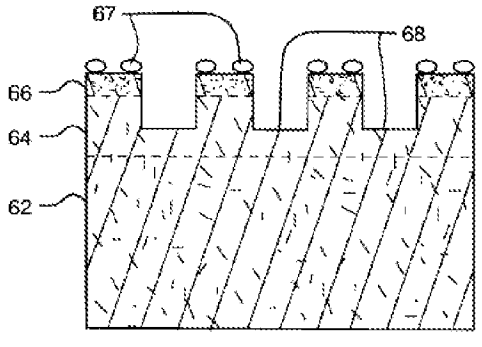

FIG. 4

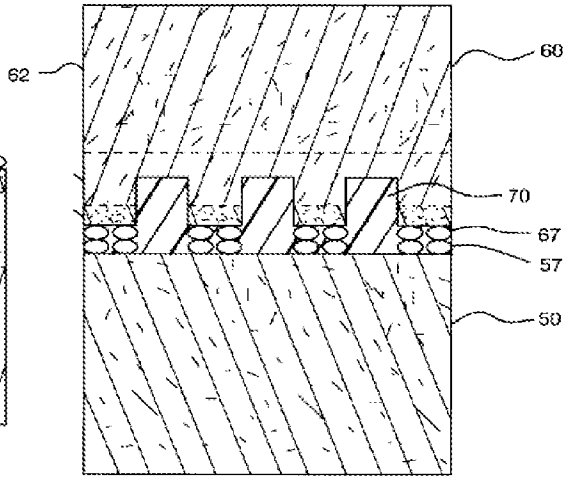

FIG. 5

Element 68, which may be considered to represent a trench, does not extend "into the common substrate from a second side of the common substrate opposite the first side of the common substrate" as claimed. Rather, trench 68 extends from the first side of the substrate 64 (where the optical devices 64, 66 are grown) toward the second side. Thus, neither of the references discloses, teaches, or suggests grouping trenches that extend from a side of a substrate opposite the side on which devices are formed or grown.

On page 3 of the final Office Action, the Examiner further referred to various elements labeled with reference numerals 50, 70, 72 of Williams '949 as the "common substrate." Applicant respectfully disagrees. As clearly shown in Fig. 6 (reproduced below), element 72 is not a substrate, but is a standoff grid (see, e.g., col. 5, line 29 of Williams '949). As discussed above, element 70 is a flowable epoxy hardener material.

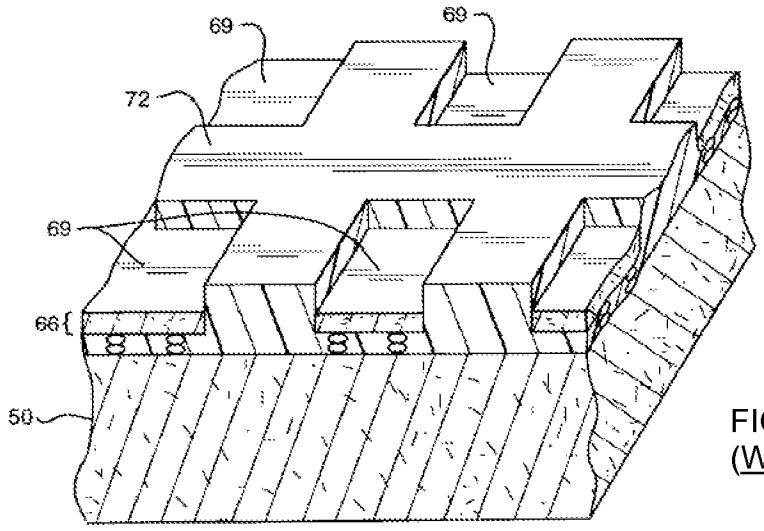

FIG. 6
(Williams '949)

Furthermore, contrary to the Examiner's assertions, the "substrate 50" is not the "common substrate" for the optical devices. Rather, the element 50 is the "ASIC substrate" to which the optical device array chip 60 is flip-chip bonded.

Moreover, Applicant respectfully submits independent Claims 1, 13, 14, 26, 42, and 52 each recite that the optical devices are "formed" on the common substrate (independent Claim 33 recites "growing…"). In contrast, the optical devices 69 in Williams '949 clearly are not "formed" or "grown" on the alleged common substrate 50.

Furthermore, amended independent Claims 1, 13, 14, 26, 33, 42, and 52 each expressly recite that the grouping trench extends into the common substrate. In contrast, the purported grouping trenches of Williams '949 do not extend into the purported substrate 50 at all.

During the interview, the Examiner suggested that Williams '949 shows trenches (as the optical devices 69 in Fig. 6 appear to be) and "grouping" of the optical devices, and thus drew the conclusion that Williams '949 teaches the "grouping trench." However, this appears to be "picking and choosing" isolated elements out of their context, and is an indication of using hindsight reconstruction to arrive at the claimed embodiment, which is impermissible. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988).

Thus, Williams '949 fails to disclose, teach, or suggest an optical module that includes "at least two optical devices . . . formed on a first side of a common substrate" and a "grouping trench" that "extends into the common substrate from a side opposite the first side of the common substrate," as recited in independent Claim 1, or similar elements recited in independent Claims 13, 14, 26, 33, 42, and 52.

Claims 6, 19, and 29 depend from independent Claims 1, 14, and 26, respectively, and thus are patentable over the cited references for at least the reasons set forth above with respect to Claims 1, 14, and 26. In addition, Claims 6, 19, and 29 each recite that "the grouping trench extends completely through the common substrate." The cited references fail to disclose, teach, or suggest at least this additional feature. Thus, Claims 6, 19, and 29 are patentable over the cited references for at least this additional reason.

Claim 57 depends from independent Claim 1 and thus is patentable over the cited references for at least the reasons set forth above with respect to Claim 1. In addition, Claim 57 recites that "the common substrate is electrically conductive, and wherein the carrier movement [between the optical devices in the group] is through the electrically conductive common substrate." On page 10 of the final Office Action, the Examiner asserted that Williams '157 teaches in col. 1, lines 25-50 that "the common substrate is electrically conductive." Applicant respectfully disagrees. The cited portion of Williams '157 reads:

> Integrated circuit technology allows large numbers of VCSEL (Vertical Cavity Surface Emitting Laser) laser emitter optical transmitters and p-i-n diode photo detector optical receivers to be constructed as large, two dimensional planar arrays, with one or more such arrays mounted on a common ASIC (Application Specific Integrated Circuit) substrate, as by flip-chip methods, also known as hybridization mounting techniques, each emitter and/or detector of the array making electrical connections with circuitry previously constructed in the ASIC substrate. This compound device, when coupled with precision alignment to a terminal end or node of a multi-channel optical link such as the end of a fiber optic bundle, provides an electro/optical communications interface where an electronic signal is converted by a VCSEL to an optical signal, directed at a end face of a single channel optical core of a terminator/connector, and hence along an optical transmission path fiber within the bundle, to be discharged via a carefully aligned receiving end fiber terminator/connector into a photo diode opto-electronic receiver on the same or another optical array of the same or another ASIC substrate, and converted by that photo detector back into an electronic signal. Fiberoptic communications channels provide significantly greater speed and effective bandwidth capabilities as compared to electrically conductive leads.

However, in the above paragraph and, in fact, throughout the disclosures of Williams '157 and Williams '949, there is nothing teaching or suggesting that "the common substrate is electrically conductive," or that "the carrier movement [between the optical devices in the group] is through the electrically conductive common substrate." If the Examiner had equated the ASIC substrate to the "common substrate" as claimed, Applicant respectfully submits that an electrically conductive ASIC substrate would short out the electrical elements on

the ASIC substrate. Furthermore, as the ASIC chip processes the electrical signals from the optical devices, there is no reason to believe that the ASIC chip would allow "carrier movement" between the optical devices.

Thus, Claim 57 is patentable over the cited references for at these additional reasons.

In view of the above, independent Claims 1, 13, 14, 26, 33, 42, and 52 and their respectively associated dependent claims are patentable over Williams '157 and Williams '949. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of Claims 1-34 and 42-61.

* * *

It is submitted that each outstanding objection and rejection to the Application has been overcome, and that the Application is in a condition for allowance. Applicant respectfully requests consideration and allowance of all pending claims.

It should also be noted that although arguments have been presented with respect to certain claims herein, the recited subject matter as well as various other subject matter and/or combinations of subject matter may be patentable for other reasons. Further, the failure to address any statement by the Examiner herein should not be interpreted as acquiescence or agreement with such statement. Applicant expressly reserves the right to set forth additional and/or alternative reasons for patentability and/or allowance with the present Application or in any other future proceeding, and to rebut any statement presented by the Examiner in this or other papers during prosecution of the present Application.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present Application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this Application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to

Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by the credit card payment instructions in EFS-Web being incorrect or absent, resulting in a rejected or incorrect credit card transaction, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extension of time is needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. § 1.136 and authorizes payment of any such extension fee to Deposit Account No. 19-0741.

Respectfully submitted,

Date: January 5, 2010

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